



Genesys Logic, Inc.

GL850G

**USB 2.0
HUB Controller**

**Datasheet
Revision 1.04
Aug. 08, 2007**



Copyright:

Copyright © 2007 Genesys Logic Incorporated. All rights reserved. No part of the materials may be reproduced in any form or by any means without prior written consent of Genesys Logic, Inc.

Disclaimer:

ALL MATERIALS ARE PROVIDED "AS IS" WITHOUT EXPRESS OR IMPLIED WARRANTY OF ANY KIND. NO LICENSE OR RIGHT IS GRANTED UNDER ANY PATENT OR TRADEMARK OF GENESYS LOGIC INC.. GENESYS LOGIC HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS IN REGARD TO MATERIALS, INCLUDING ALL WARRANTIES, IMPLIED OR EXPRESS, OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF INTELLECTUAL PROPERTY. IN NO EVENT SHALL GENESYS LOGIC BE LIABLE FOR ANY DAMAGES INCLUDING, WITHOUT LIMITATION, DAMAGES RESULTING FROM LOSS OF INFORMATION OR PROFITS. PLEASE BE ADVISED THAT THE MATERIALS MAY CONTAIN ERRORS OR OMMISIONS. GENESYS LOGIC MAY MAKE CHANGES TO THE MATERIALS OR TO THE PRODUCTS DESCRIBED THEREIN AT ANY TIME WITHOUT NOTICE.

Trademarks:



is a registered trademark of Genesys Logic, Inc.
All trademarks are the properties of their respective owners.

Office:

Genesys Logic, Inc.

12F, No. 205, Sec. 3, Beishin Rd., Shindian City,

Taipei, Taiwan

Tel: (886-2) 8913-1888

Fax: (886-2) 6629-6168

<http://www.genesyslogic.com>



Revision History

Revision	Date	Description
1.00	05/10/2006	First formal release
1.01	08/30/2006	Updated DC Supply Current, Table6.6, P.23
1.02	11/03/2006	Modify 93C46 Configuration, Table 5.1, P.19
1.03	01/17/2007	Modify Table 6.1-Maximum Ratings, P.21
1.04	08/08/2007	Modify Table 6.6-DC Supply Current, P.23



TABLE OF CONTENTS

CHAPTER 1	GENERAL DESCRIPTION.....	7
CHAPTER 2	FEATURES	8
CHAPTER 3	PIN ASSIGNMENT	9
3.1	PINOUTS.....	9
3.2	PIN LIST.....	10
3.3	PIN DESCRIPTIONS	10
CHAPTER 4	BLOCK DIAGRAM.....	13
CHAPTER 5	FUNCTION DESCRIPTION	14
5.1	GENERAL	14
5.2	CONFIGURATION AND I/O SETTINGS.....	16
CHAPTER 6	ELECTRICAL CHARACTERISTICS.....	21
6.1	MAXIMUM RATINGS.....	21
6.2	OPERATING RANGES.....	21
6.3	DC CHARACTERISTICS	21
6.4	POWER CONSUMPTION	23
CHAPTER 7	PACKAGE DIMENSION.....	24
CHAPTER 8	ORDERING INFORMATION	25

LIST OF FIGURES

FIGURE 3.1 – GL850G 48 PIN LQFP PINOUT DIAGRAM..... 9

FIGURE 4.1 – GL850G BLOCK DIAGRAM (SINGLE TT) 13

FIGURE 5.1 – OPERATING IN USB 1.1 SCHEME..... 15

FIGURE 5.2 – OPERATING IN USB 2.0 SCHEME..... 16

FIGURE 5.3 – POWER ON SEQUENCE OF GL850G..... 17

FIGURE 5.4 – TIMING OF PGANG/SUSPEND STRAPPING 17

FIGURE 5.5 – INDIVIDUAL/GANG MODE SETTING 18

FIGURE 5.6 – SELF/BUS POWER SETTING 18

FIGURE 5.7 – LED CONNECTION 19

FIGURE 5.8 – SCHEMATICS BETWEEN GL850G AND 93C46..... 20

FIGURE 7.1 – GL850G 48 PIN LQFP PACKAGE..... 24



LIST OF TABLES

TABLE 3.1 – GL850G 48 PIN LIST	10
TABLE 3.3 - PIN DESCRIPTIONS	10
TABLE 5.1 – 93C46 CONFIGURATION	19
TABLE 6.1 – MAXIMUM RATINGS.....	21
TABLE 6.2 – OPERATING RANGES	21
TABLE 6.3 – DC CHARACTERISTICS EXCEPT USB SIGNALS.....	21
TABLE 6.4 – DC CHARACTERISTICS OF USB SIGNALS UNDER FS/LS MODE	22
TABLE 6.5 – DC CHARACTERISTICS OF USB SIGNALS UNDER HS MODE	22
TABLE 6.6 – DC SUPPLY CURRENT	23
TABLE 8.1 – ORDERING INFORMATION.....	25



CHAPTER 1 GENERAL DESCRIPTION

GL850G is Genesys Logic's advanced version Hub solutions which fully comply with Universal Serial Bus Specification Revision 2.0.

GL850G embeds an 8-bit RISC processor to manipulate the control/status registers and respond to the requests from USB host. Firmware of GL850G will control its general purpose I/O (GPIO) to access the external EEPROM and then respond to the host the customized PID and VID configured in the external EEPROM. Default settings in the internal mask ROM is responded to the host without having external EEPROM. GL850G is designed for customers with much flexibility. The more complicated settings such as PID, VID, and number of downstream ports settings are easily achieved by programming the external EEPROM (Ref. to Chapter 5).

Each downstream port of GL850G supports two-color (green/amber) status LEDs to indicate normal/abnormal status. GL850G also support both Individual and Gang modes (4 ports as a group) for power management. The GL850G is a full function solution which supports both Individual/Gang power management modes and the two-color (green/amber) status LEDs. Please refer the table in the end of this chapter for more detail.

To fully meet the cost/performance requirement, GL850G is a single TT hub solution for the cost requirement. Genesys Logic also provides GL852 for multiple TT hub solution to target on systems which require higher performance for full/low-speed devices, like docking station, embedded system ... etc.. Please refer to GL852 datasheet for more detailed information.

*TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.



CHAPTER 2 FEATURES

- Compliant to USB specification Revision 2.0
 - Support 4/3/2 downstream ports by I/O pin configuration
 - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
 - Downstream ports support HS, FS, and low-speed (LS) traffic
 - 1 control pipe (endpoint 0, 64-byte data payload) and 1 interrupt pipe (endpoint 1, 1-byte data payload)
 - Backward compatible to *USB specification Revision 1.1*
- On-chip 8-bit micro-processor
 - RISC-like architecture
 - USB optimized instruction set
 - Performance: 6 MIPS @ 12MHz
 - With 64-byte RAM and 2K mask ROM
 - Support customized PID, VID by reading external EEPROM
 - Support downstream port configuration by reading external EEPROM
- Single Transaction Translator (STT)
 - Single TT shares the same TT control logics for all downstream port devices. This is the most cost effective solution for TT. Multiple TT provides individual TT control logics for each downstream port. This is a performance better choice for USB 2.0 hub. Please refer to GL852 datasheet for more detailed information.
- Integrate USB 2.0 transceiver
- Each downstream port supports two-color status indicator, with automatic and manual modes compliant to USB specification Revision 2.0
- Built-in upstream 1.5K Ω pull-up and downstream 15K Ω pull-down
- Embed serial resistor for USB signals
- Support both individual and gang modes of power management and over-current detection for downstream ports
- Conform to bus power requirements
- Automatic switching between self-powered and bus-powered modes
- Support compound-device (non-removable in downstream ports) by I/O pin configuration
- Configurable non-removable device support
- PLL embedded with external 12 MHz crystal
- Embeds 5V to 3.3V regulator
- Low power consumption
- Improve output drivers with slew-rate control for EMI reduction
- Internal power-fail detection for ESD recovery
- Full function in 48-pin LQFP package
- Applications:
 - Stand-alone USB hub
 - PC motherboard USB hub, Docking of notebook
 - LCD monitor hub
 - Any compound device to support USB HUB function

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

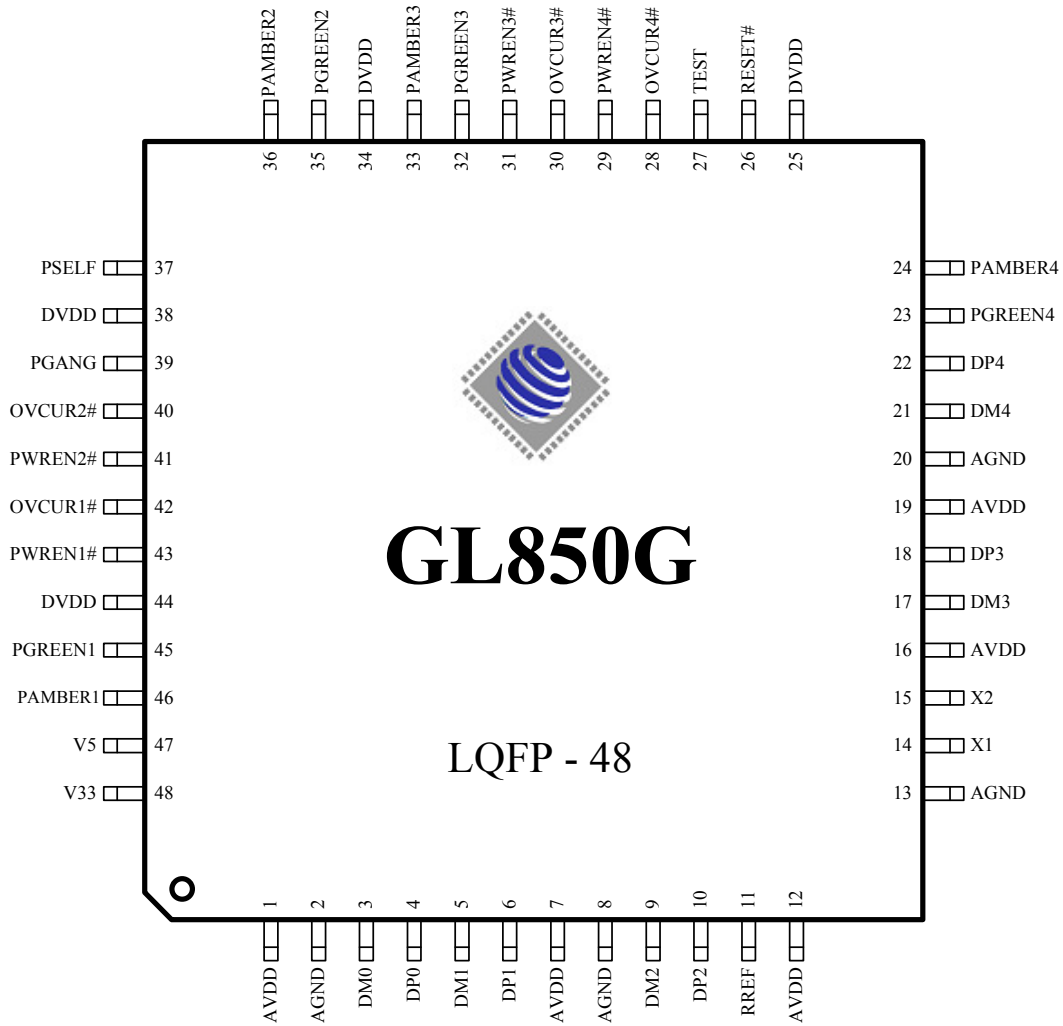


Figure 3.1—GL850G 48 Pin LQFP Pinout Diagram

3.2 Pin List

Table 3.1 – GL850G 48 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVDD	P	13	AGND	P	25	DVDD	P	37	PSELF	I_5V
2	AGND	P	14	X1	I	26	RESET#	I_5V	38	DVDD	P
3	DM0	B	15	X2	O	27	TEST	I	39	PGANG	B
4	DP0	B	16	AVDD	P	28	OVCUR4#	I_5V	40	OVCUR2#	I_5V
5	DM1	B	17	DM3	B	29	PWREN4#	O	41	PWREN2#	O
6	DP1	B	18	DP3	B	30	OVCUR3#	I_5V	42	OVCUR1#	I_5V
7	AVDD	P	19	AVDD	P	31	PWREN3#	O	43	PWREN1#	O
8	AGND	P	20	AGND	P	32	PGREEN3	O	44	DVDD	P
9	DM2	B	21	DM4	B	33	PAMBER3	O	45	PGREEN1	O
10	DP2	B	22	DP4	B	34	DVDD	P	46	PAMBER1	O
11	RREF	B	23	PGREEN4	O	35	PGREEN2	B	47	V5	P
12	AVDD	P	24	PAMBER4	O	36	PAMBER2	O	48	V33	P

3.3 Pin Descriptions

Table 3.3 - Pin Descriptions

USB Interface			
Pin Name	GL850G	I/O Type	Description
	48Pin#		
DM0,DP0	3,4	B	USB signals for USPORT
DM1,DP1	5,6	B	USB signals for DSPORT1
DM2,DP2	9,10	B	USB signals for DSPORT2
DM3,DP3	17,18	B	USB signals for DSPORT3
DM4,DP4	21,22	B	USB signals for DSPORT4
RREF	11	B	A 680Ω resistor must be connected between RREF and analog ground (AGND).

Note: USB signals must be carefully handled in PCB routing. For detailed information, please refer to **GL850G Design Guideline**.

HUB Interface			
Pin Name	GL850G	I/O Type	Description
	48Pin#		
OVCUR1~4#	42,40, 30,28	I_5V (pu)	Active low. Over current indicator for DSPORT1~4 OVCUR1# is the only over current flag for GANG mode.
PWREN1~4#	43,41, 31,29	O	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode.
PGREEN1~4	45,35, 32,23	1,3,4:O 2:B (pd)	Green LED indicator for DSPORT1~4 *GREEN[1~2] are also used to access the external EEPROM For detailed information, please refer to Chapter 5.
PAMBER1~4	46,36, 33,24	O (pd)	Amber LED indicator for DSPORT1~4 *Amber[1~2] are also used to access the external EEPROM For detailed information, please refer to Chapter 5.
PSELF	37	I_5V	0: GL850G is bus-powered. 1: GL850G is self-powered.
PGANG	39	B	This pin is default put in input mode after power-on reset. Individual/gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When GL850G is suspended, this pin will output low. *For detailed explanation, please see Chapter 5 Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend

Clock and Reset Interface			
Pin Name	GL850G	I/O Type	Description
	48Pin#		
X1	14	I	12MHz crystal clock input.
X2	15	O	12MHz crystal clock output.
RESET#	26	I_5V	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.

System Interface			
Pin Name	GL850G	I/O Type	Description
	48Pin#		
TEST	27	I (pd)	0: Normal operation. 1: Chip will be put in test mode.

Power / Ground			
Pin Name	GL850G	I/O Type	Description
	48Pin#		
AVDD	1,7,12, 16,19	P	3.3V analog power input for analog circuits.
AGND	2,8,13, 20	P	Analog ground input for analog circuits.



DVDD	25,34, 38,44	P	3.3V digital power input for digital circuits
V5	47	P	5V-to-3.3V regulator Vin
V33	48	P	5V-to-3.3V regulator Vout

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **GL850G Design Guideline**.

Notation:

Type	O	Output
	I	Input
	I_5V	5V tolerant input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

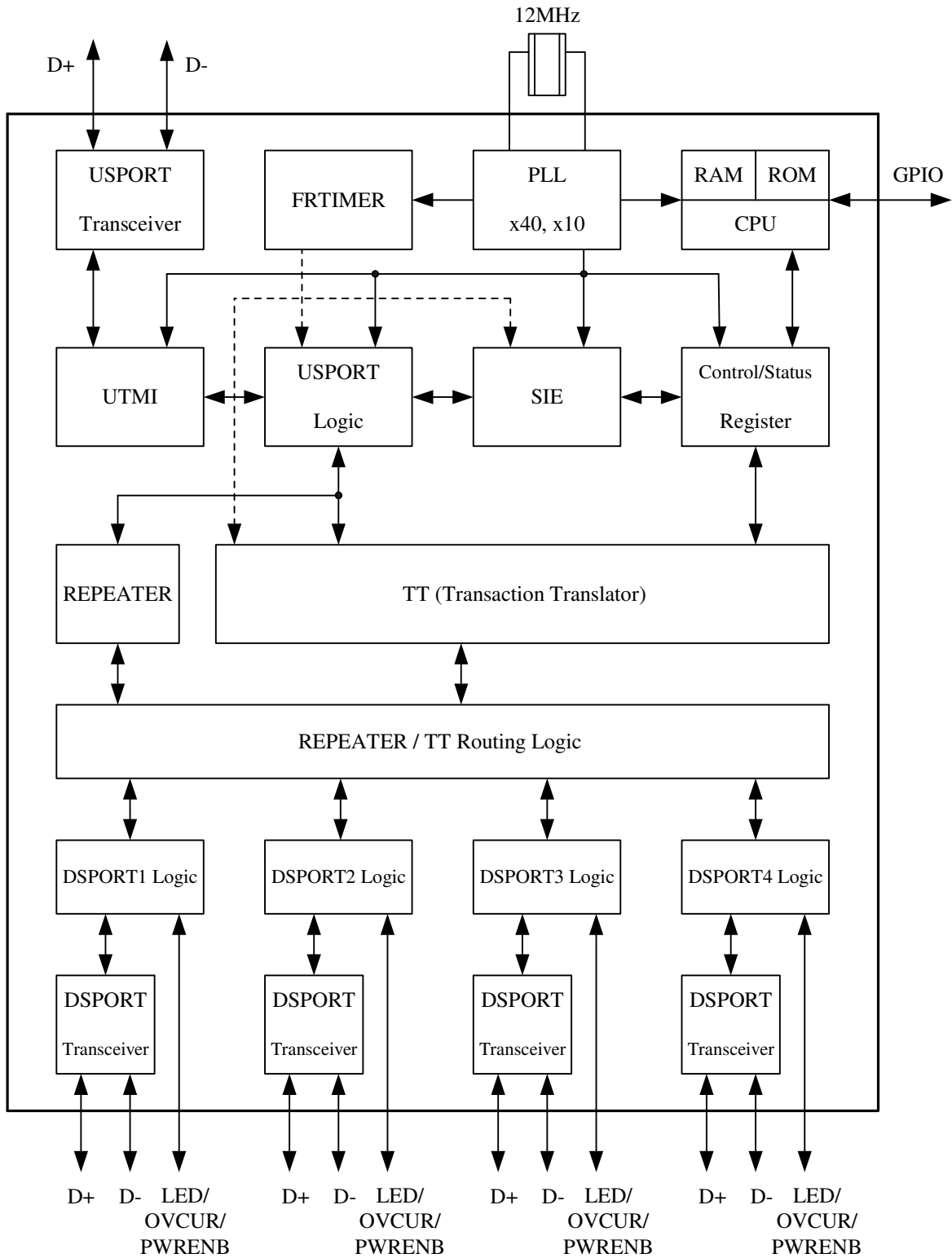


Figure 4.1 – GL850G Block Diagram (single TT)



CHAPTER 5 FUNCTION DESCRIPTION

5.1 General

5.1.1 USPORT Transceiver

USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. USPORT transceiver will operate in full-speed electrical signaling when GL850G is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL850G is plugged into a 2.0 host/hub.

5.1.2 PLL (Phase Lock Loop)

GL850G contains a 40x PLL. PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

5.1.3 FRTIMER

This module implements hub (micro)frame timer. The (micro)frame timer is derived from the hub's local clock and is synchronized to the host (micro)frame period by the host generated Start of (micro)frame (SOF). FRTIMER keeps tracking the host's SOF such that GL850G is always safely synchronized to the host. The functionality of FRTIMER is described in section 11.2 of *USB Specification Revision 2.0*.

5.1.4 μ C

μ C is the micro-processor unit of GL850G. It is an 8-bit RISC processor with 2K ROM and 64 bytes RAM. It operates at 6MIPS of 12Mhz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, μ C can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of hub. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.

5.1.5 UTMI (USB 2.0 Transceiver Macrocell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

5.1.6 USPORT logic

USPORT implements the upstream port logic defined in section 11.6 of *USB specification Revision 2.0*. It mainly manipulates traffics in the upstream direction. The main functions include the state machines of Receiver and Transmitter, interfaces between UTMI and SIE, and traffic control to/from the REPEATER and TT.

5.1.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0*. It co-works with μ C to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

5.1.8 Control/Status register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL850G possesses higher flexibility to control the USB protocol easily and correctly.

5.1.9 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of *USB specification Revision 2.0*. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

5.1.10. TT (Transaction Translator)

TT implements the control logic defined in section 11.14 ~ 11.22 of *USB specification Revision 2.0*. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL850G adopts the single TT architecture to provide the most cost effective solution. Single TT shares the same buffer control module for each downstream port. GL852 adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively. Please refer to GL852 datasheet for more detailed information.

5.1.11 REPEATER/TT routing logic

REPEATER and TT are the major traffic control machines in the USB 2.0 hub. Under situation that USPORT and DSPORT are signaling in the same speed, REPEATER/TT routing logic switches the traffic channel to the REPEATER. Under situation that USPORT is in the high speed signaling and DSPORT is in the full/low speed signaling, REPEATER/TT routing logic switches the traffic channel to the TT.

5.1.11.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

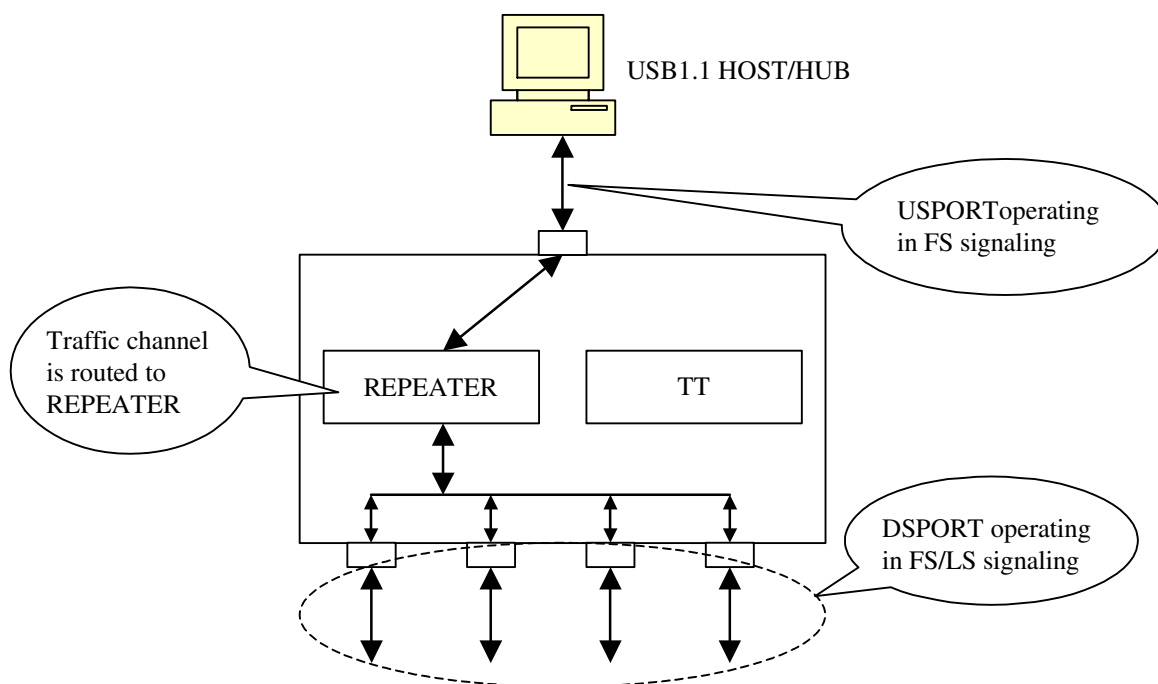


Figure 5.1 – Operating in USB 1.1 scheme

5.1.11.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

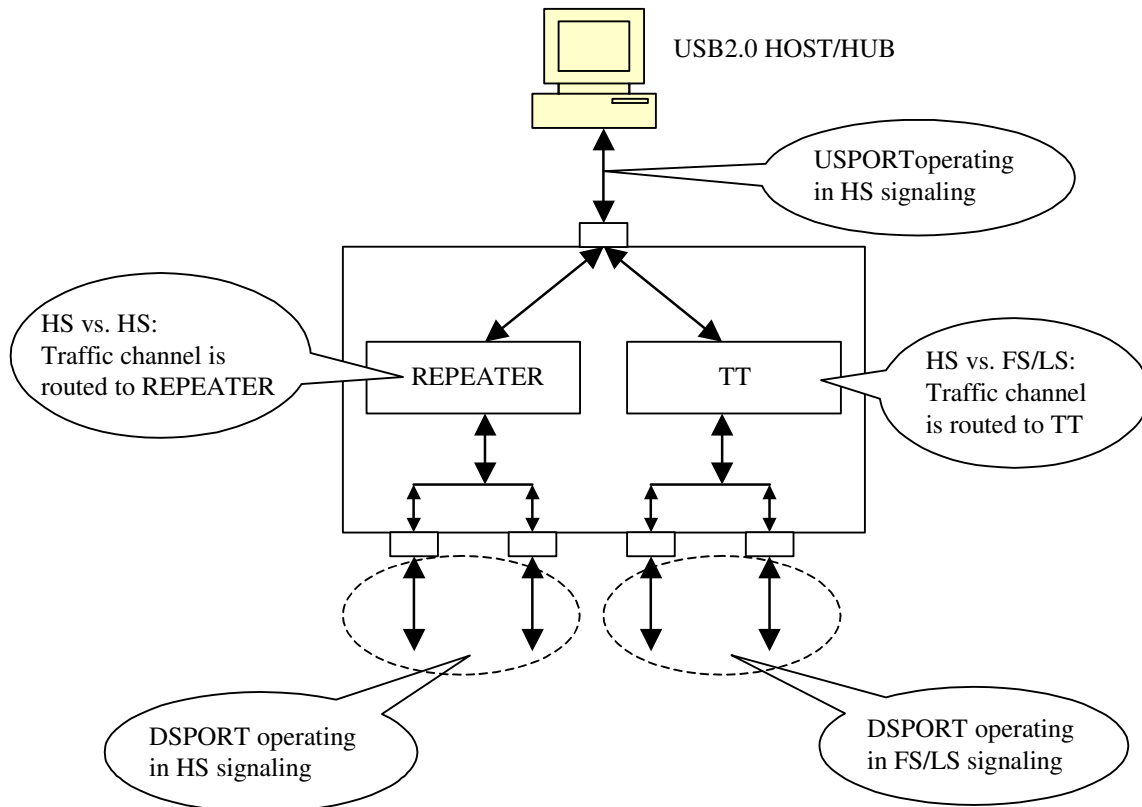


Figure 5.2 – Operating in USB 2.0 scheme

5.12 DSPORT logic

DSPORT (downstream port) logic implements the control logic defined in section 11.5 of *USB specification Revision 2.0*. It mainly manipulates the state machine, the connection/disconnection detection, over current detection and power enable control, and the status LED control of the downstream port. Besides, it also output the control signals to the DSPORT transceiver.

5.13 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

5.2 Configuration and I/O Settings

5.2.1 RESET# Setting

GL850G integrates in the pull-up 15K Ω resistor of the upstream port. When RESET# is enabled, the internal 15K Ω pull-up resistor will be disconnected to the 3.3V power. To meet the requirement (p.141) of the USB 2.0 specification, pull-up resistor should be disconnected while lacking of USB cable power (Vbus).

GL850G internally contains a power on reset circuit. The power on sequence is depicted in the next picture. To fully control the reset process of GL850G, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit.

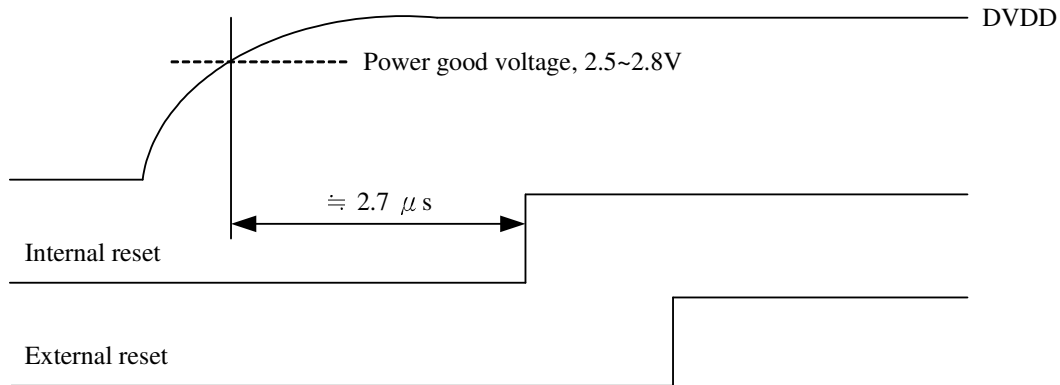


Figure 5.3 – Power on sequence of GL850G

5.2.2 PGANG/SUSPND Setting

To save pin count, GL850G uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 20us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL850G outputs the suspend flag once it is globally suspended. For individual mode, a pull low resistor greater than 100KΩ should be placed. For gang mode, a pull high resistor greater than 100KΩ should be placed. In figure 5.5, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

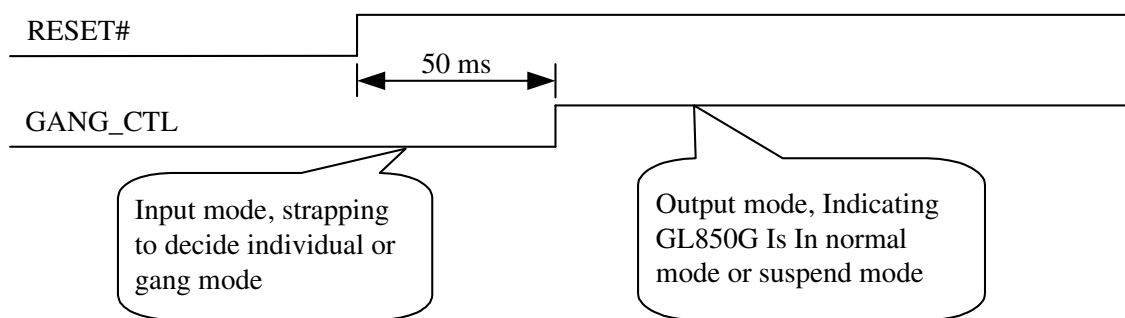


Figure 5.4 – Timing of PGANG/SUSPEND strapping

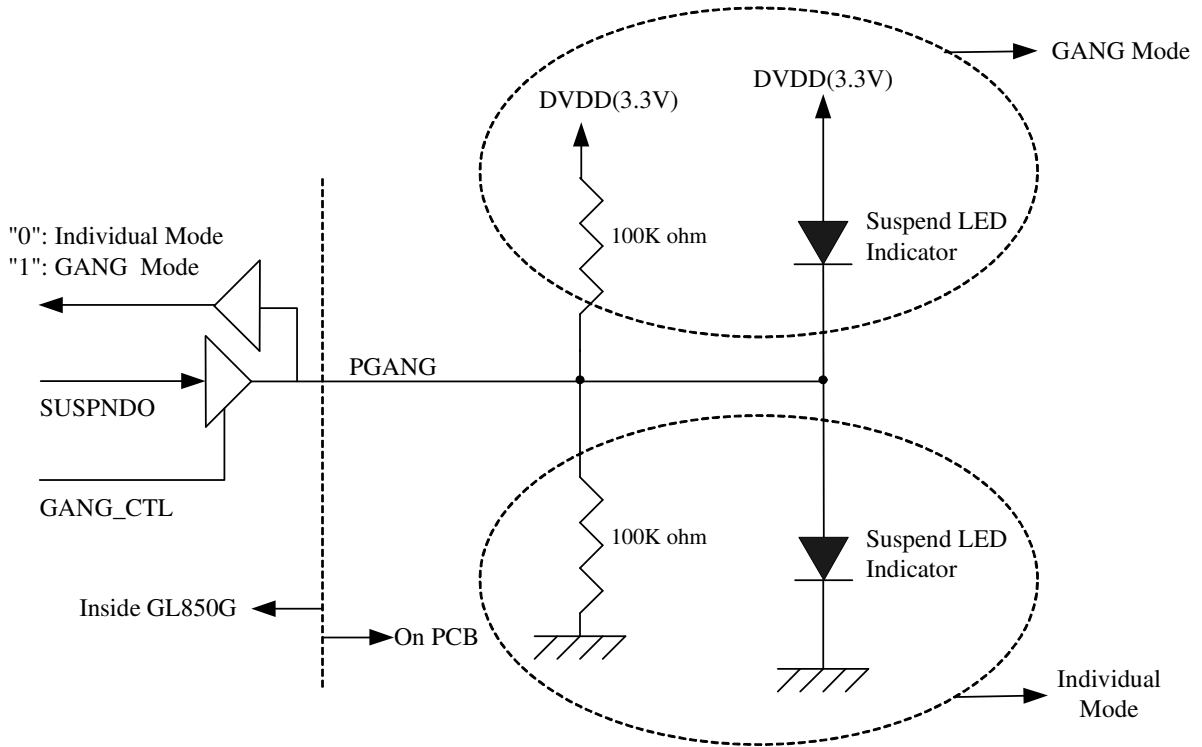


Figure 5.5 – Individual/GANG Mode Setting

5.2.3 SELF/BUS Power Setting

GL850G can operate under bus power and conform to the power consumption limitation completely (suspend current < 2.5 mA, normal operation current < 100 mA). By setting PSELF, GL850G can be configured as a bus-power or a self-power hub.

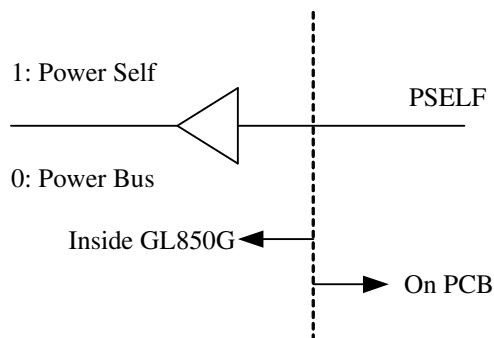


Figure 5.6 – SELF/BUS Power Setting

5.2.4 LED Connections

GL850G controls the LED lighting according to the flow defined in section 11.5.3 of *Universal Serial Bus Specification Revision2.0*. Both manual mode and Automatic mode are supported in GL850G. When GL850G is globally suspended, GL850G will turn off the LED to save power.

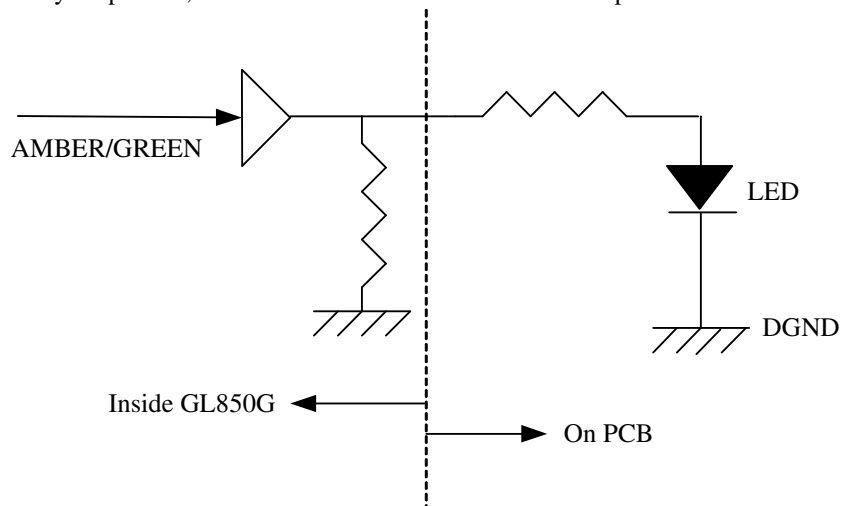


Figure 5.7 – LED Connection

5.2.5 EEPROM Setting

GL850G replies to host commands by the default settings in the internal ROM. GL850G also offers the ability to reply to the host according to the settings in the external EEPROM(93C46). The following table shows the configuration of 93C46.

Table 5.1 – 93C46 Configuration

Unit: Byte

	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
00h	VID_L	VID_H	PID_L	PID_H	CHKSUM	FF	DEVICE REMOVABLE	PORT NUMBER	MaxPower	FF	FF	FF	FF	FF	FF	FF	
10h	VENDOR LENGTH	→start															
20h	Vendor string (ASC II code)																
30h	end																
40h	PRODUCT LENGTH	→start															
50h	Product String(ASC II code)																
60h	end																
70h	SERIAL NUMBER LENGTH	→ start														Serial Number String(ASC II code)	
		end															

- Note: 1. VID_H/VID_L: high/low byte of VID value
 2. PID_H/PID_L: high/low byte of PID value
 3. CHKSUM: CHKSUM must equal to VID_H + VID_L + PID_H + PID_L + 1, otherwise firmware will ignore the EEPROM settings.
 4. PORT_NO: port number, value must be 1~4.
 5. MaxPower : Describe the maximum power consumption, range=0Ma~500Ma . Value -> 00H~FAH (unit = 2Ma)
 6. DEVICE REMOVALBE:

-	-	-	PORT4 REMOVABLE	PORT3 REMOVABLE	PORT2 REMOVABLE	PORT1 REMOVABLE	-
---	---	---	--------------------	--------------------	--------------------	--------------------	---

- 0: Device attached to this port is removable.
 1: Device attached to this port is non-removable.

7. VENDOR LENGTH: offset 10h contains the length of the vendor string. Values of vendor string is contained from 11h~3Fh.
 8. PRODUCT LENGTH: offset 40h contains the length of product string. Values of product string is contained from 41h~6Fh.
 9. SERIAL NUMBER LENGTH: offset 70h contains the value of serial number string. Values of serial number string is contained after offset 71h.

The schematics between GL850G and 93C46 is depicted in the following figures:

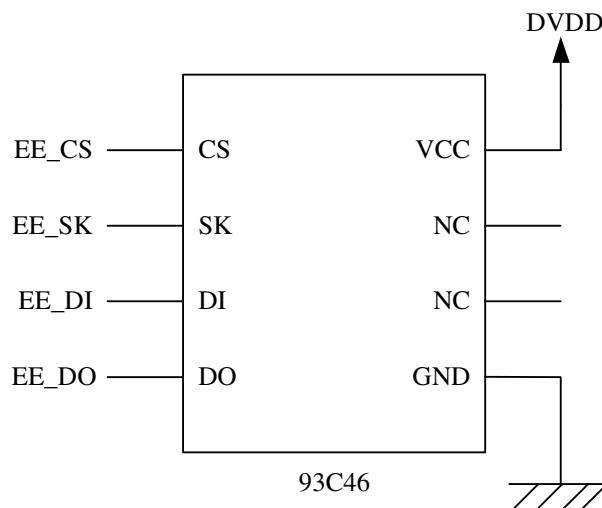


Figure 5.8 – Schematics Between GL850G and 93C46

GL850G firstly verifies the check sum after power on reset. If the check sum is correct, GL850G will take the configuration of 93C46 as part of the descriptor contents. To prevent the content of 93C46 from being over-written, amber LED will be disabled when 93C46 exists.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 – Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V ₅	5V Power Supply	-0.5	+6.0	V
V _{DD}	3.3V Power Supply	-0.5	+3.6	V
V _{IN}	Input Voltage for digital I/O pins	-0.5	+3.6	V
V _{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	+5.5	V
V _{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T _S	Storage Temperature under bias	-55	+100	°C
F _{OSC}	Frequency	12 MHz ± 0.05%		

6.2 Operating Ranges

Table 6.2 – Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V ₅	5V Power Supply	4.5	5.0	5.5	V
V _{DD}	3.3V Power Supply	3.15	3.3	3.45	V
V _{IND}	Input Voltage for digital I/O pins	-0.5		3.6	V
V _{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5		5.0	V
V _{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5		3.6	V
T _A	Ambient Temperature	0		70	°C

6.3 DC Characteristics

Table 6.3 – DC Characteristics Except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
P _D	Power Dissipation	70	-	180	mA
V ₃₃	5V to 3.3V regulator output with 200mA load	2.9	3.3	3.52	V
V _{IL}	LOW level input voltage	-	-	0.8	V
V _{IH}	HIGH level input voltage	2.0	-	-	V
V _{TLH}	LOW to HIGH threshold voltage	1.4	1.5	1.6	V
V _{THL}	HIGH to LOW threshold voltage	0.87	0.94	0.99	V
V _{OL}	LOW level output voltage when I _{OL} =8mA	-	-	0.4	V
V _{OH}	HIGH level output voltage when I _{OH} =8mA	2.4	-	-	V
R _{DN}	Pad internal pull down resister	29	59	135	KΩ
R _{UP}	Pad internal pull up resister	80	108	140	KΩ

Table 6.4 – DC Characteristics of USB Signals Under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{OL}	DP/DM FS static output LOW(R _L of 1.5K to 3.6V)	0	-	0.1	V
V _{OH}	DP/DM FS static output HIGH (R _L of 15K to GND)	2.8	-	3.6	V
V _{DI}	Differential input sensitivity	0.2	-	-	V
V _{CM}	Differential common mode range	0.8	-	2.5	V
V _{SE}	Single-ended receiver threshold	0.2	-	-	V
C _{IN}	Transceiver capacitance	-	-	20	Pf
I _{LO}	Hi-Z state data line leakage	-10	-	+10	μA
Z _{DRV}	Driver output resistance	42	45	48	Ω

Table 6.5 – DC Characteristics of USB Signals Under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{OL}	DP/DM HS static output LOW(R _L of 1.5K to 3.6V)	-	-	0.1	V
C _{IN}	Transceiver capacitance	4	4.5	5	Pf
I _{LO}	Hi-Z state data line leakage	-5	0	+5	μA
Z _{DRV}	Driver output resistance for USB 2.0 HS	42	45	48	Ω

6.4 Power Consumption

Table 6.6 – DC Supply Current

Symbol	Condition			Typ.	Unit
	Active ports	Host	Device		
I_{SUSP}	Suspend			1.1	mA
I_{CC}	4	F*1	F	94	mA
		H*1	H	178	mA
		H	F	114	mA
	3	F	F	91	mA
		H	H	160	mA
		H	F	110	mA
	2	F	F	87	mA
		H	H	141	mA
		H	F	106	mA
	1	F	F	84	mA
		H	H	120	mA
		H	F	102	mA
	No Active	F		80	mA
		H		97	mA

*1: F: Full-Speed, H: High-Speed



CHAPTER 8 ORDERING INFORMATION

Table 8.1 – Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL850G-MNNXX	48-pin LQFP	Normal Package	XX	
GL850G-MNGXX	48-pin LQFP	Green Package	XX	